

Europäisches Patentamt
European Patent Office
Office européen des brevets



(11) EP 1 156 490 A1

(12)

EUROPEAN PATENT APPLICATION
published in accordance with Art. 158(3) EPC

(43) Date of publication:
21.11.2001 Bulletin 2001/47

(21) Application number: 00964674.6

(22) Date of filing: 04.10.2000

(51) Int Cl.7: G11C 17/00, B41J 2/175

(86) International application number:
PCT/JP00/06935

(87) International publication number:
WO 01/26115 (12.04.2001 Gazette 2001/15)

(84) Designated Contracting States:
AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU
MC NL PT SE
Designated Extension States:
AL LT LV MK RO SI

(30) Priority: 04.10.1999 JP 28324599

(71) Applicant: SEIKO EPSON CORPORATION
Shinjuku-ku, Tokyo 163-0811 (JP)

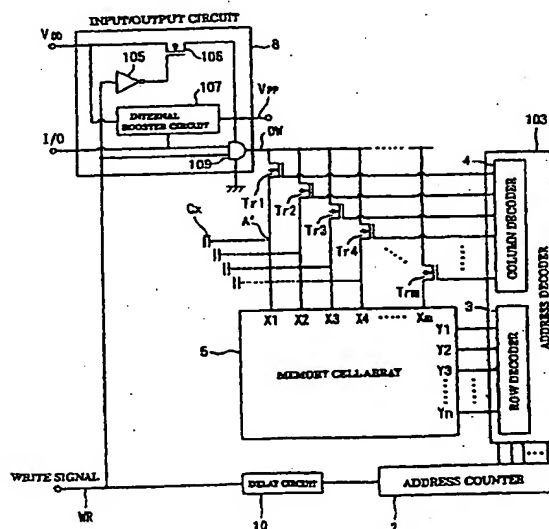
(72) Inventor: TAKAGI, Tetsuo
Suwa-shi, Nagano-ken 392-8502 (JP)

(74) Representative: Hoffmann, Eckart, Dipl.-Ing.
Patentanwalt,
Bahnhofstrasse 103
82166 Gräfelfing (DE)

(54) SEMICONDUCTOR INTEGRATED CIRCUIT, INK CARTRIDGE HAVING THIS SEMICONDUCTOR INTEGRATED CIRCUIT, AND INK JET RECORDING DEVICE MOUNTED WITH THIS INK CARTRIDGE

(57) A signal line is charged in a short time and surely in a semiconductor integrated circuit including a charge unit for charging a signal line corresponding to each 1 row in response to an input of a writing instruction for each bit of a memory cell arranged in n rows by m columns (where n and m are natural numbers and so forth) and charging a signal line corresponding to a next row after writing on all bits for one column is completed, and performing writing on each 1 bit sequentially in each of bits for 1 column corresponding to the signal line charged by the charge unit. By having a delay unit, a time for discharging charges charged in a parasitic capacity is reserved. An address is changed after the discharge is completed so that wrong writing does not occur.

FIG. 1



Description

Technical Field

[0001] The present invention relates to a semiconductor integrated circuit, an ink cartridge having the semiconductor integrated circuit, and an inkjet recording device having the ink-cartridge attached, more particularly, to a semiconductor integrated circuit having a non-volatile memory built in and using boosted voltage for data writing, an ink cartridge having the semiconductor integrated circuit, and an inkjet recording device having the ink cartridge attached.

Background Art

[0002] Conventionally, such a semiconductor integrated circuit performs a write operation by using voltage boosted by an internal booster circuit when writing data to a built-in, non-volatile memory. At the end of writing, charges integrated in a signal line charged at the time of writing is discharged before shifting to the next writing operation. In this case, the discharging is performed by a discharge circuit within the semiconductor integrated circuit.

[0003] Fig. 13 is a circuit diagram showing a discharge circuit in a conventional semiconductor integrated circuit. As shown in Fig. 14, the discharge circuit discharges charges integrated in a parasitic capacity C_x associated with a signal line to a memory cell array 5. The parasitic capacity C_x is charged in the following manner: An address counter 2 performs a count operation in response to an input of a write signal WR so that an address decoder whose input is the count value operates. The address decoder 103 includes a column decoder 4 and a row decoder 3 for specifying a column and a row of memory cells forming a memory cell array 5, respectively. The memory cell array 5 includes a plurality of memory cells arranged in n rows by m columns.

[0004] Each of outputs of the column decoder 4, that is the decoded result, is input to respective gate terminals of transistors Tr_1, Tr_2, \dots and Tr_m which are switching elements. The source terminal of each transistor is connected to a data wire DW while the drain terminal is connected to a signal line corresponding to a respective column of memory cells in the memory cell array 5. Therefore, by turning any one of transistors Tr_1, Tr_2, \dots and Tr_m to the ON status with the output of the column decoder 4, a signal line corresponding to a respective column is charged by voltage of the data wire DW through the respective transistor. In other words, charges are integrated in a parasitic capacity of the signal line corresponding to the column specified by the column decoder 4. For example, when the transistor Tr_1 is turned ON, charges are integrated in the parasitic capacity of the signal line including a node A.

[0005] Here, the output of an input/output control circuit 8 is supplied to the data wire DW. The input/output

control circuit 8 includes an internal booster circuit 107 for boosting the voltage of a power supply V_{DD} in response to an input of the write signal WR, an inverter for generating an inverted signal of the write signal WR, a switching transistor 106 to whose gate terminal is supplied with the output of the inverter 105, that is the inverted signal of the write signal WR, and a buffer 108 having a boosted output V_{PP} as a power supply and supplying voltage corresponding to a value of a data input I/O to the data wire DW.

[0006] In the discharge circuit 101 having such a construction, the write signal WR is at high level when writing to a memory cell while the transistor 106 is in the OFF condition. Here, the power supply V_{DD} is supplied to the internal booster circuit 107, resulting in a higher potential (15 volt, for example) of the boosted output V_{PP} . The potential is supplied to the buffer 108 as a power supply. Thus, voltage corresponding to a value of the data input I/O is supplied from the buffer 108 to the data wire DW. In this condition, turning any one of the transistors Tr_1, Tr_2, \dots to the ON condition, a signal wire corresponding to the respective column is charged by the voltage of the data wire DW through the transistor. In the condition where the signal line is charged (the condition where charges are integrated), data is written in each one of memory cells within the memory cell array 5 by the sequential changes in the outputs of the row decoder 3.

[0007] On the other hand, at the time of reading from the memory cells or at another time, the write signal WR is at the low level, and the transistor 106 is turned ON. At this time, the power supply V_{DD} is not supplied to the internal booster circuit 107, which turns the boosted output V_{PP} to the low potential (5 volt, for example). The output of the buffer 108 to which the potential is supplied as the power supply is turned to the low level regardless of the value of the data input I/O. Therefore, the above-described integrated charges are discharged through the data wire DW to which the output of the buffer 108 is supplied. For example, the charges integrated in the parasitic capacity C_x at node A shown are discharged toward ground applied to the buffer 108.

[0008] In short, in the conventional discharge circuit 101, by turning the transistor 106 to the ON condition at the time the writing ends, the integrated charges are discharged. However, in the semiconductor integrated circuit having such a discharge circuit, there are problems as follows:

[0009] First of all, it takes time for removing the charges completely. Thus, there is a problem that a certain amount of time is required before writing on a next memory cell.

[0010] Further, when the count value of the address counter varies at the time the writing ends, charges with higher voltage remain in the parasitic capacity, which may be a factor for the residual charges to cause wrong writing. The wrong writing will be described with reference to Fig. 14.

[0011] In the figure, when writing to the X1 column of memory cells, the transistor Tr1 is turned ON by the column decoder 4, first of all, and the parasitic capacity Cx at node A is charged. In the charged condition, writing is performed by the row decoder 3 in the sequence of row Y1, row Y2...to row Yn. When the writing is completed at row Yn, the parasitic capacity Cx is discharged as described above. After the discharging, the transistor Tr2 corresponding to a next column X2 is turned ON by the column decoder 4, and the next parasitic capacity Cx is charged. In the charged condition, writing is performed by the row decoder 3 in the sequence of row Y1, row Y2...to row Yn. Charging and discharging are repeatedly performed on the other signal lines in similar manner. Through this operation, each 1 bit is specified in order from column X1 and row y1 to column Xm and row Yn, and then writing is performed on all bits included in the memory cell array 5.

[0012] In the operation above, when transition happens from writing on the row of X1, the column of Yn to the writing on the row of X2, the column of Y1, the row of Y1 may be specified regardless of a condition where discharging of the signal line of the column of X1 has not been completed. In this case, there is a problem that wrong writing is performed by remaining charges.

[0013] The present invention was made in order to overcome the problems of the above-describe conventional technology. A purpose of the present invention is to provide a semiconductor integrated circuit having a discharge circuit, which can surely discharge, an ink cartridge using it, and an inkjet recording device having the cartridge.

Disclosure of Invention

[0014] A semiconductor integrated circuit according to the present invention includes a charge unit for charging a signal line corresponding to each 1 row in response to an input of a writing instruction for each bit of a memory cell arranged in n rows by m columns (where n and m are natural numbers and so forth) and charging a signal line corresponding to a next row after writing on all bits for one column is completed. The semiconductor integrated circuit performs writing on each 1 bit sequentially in each of bits for 1 column corresponding to the signal line charged by the charge unit. Further, the semiconductor integrated circuit includes a delay unit for delaying an input of the writing instruction to the charge unit for at least a time equivalent to a discharge time for the signal line.

[0015] Another semiconductor integrated circuit according to the present invention includes a charge unit for charging a signal line corresponding to each 1 row in response to an input of a writing instruction for each bit of a memory cell arranged in n rows by m columns and charging a signal line corresponding to a next row after writing on all bits for one column is completed. The

semiconductor integrated circuit performs writing on each 1 bit sequentially in each of bits for 1 column corresponding to the signal line charged by the charge unit. Further, the semiconductor integrated circuit includes a suppressing unit for suppressing a change in address indicating a cell to be written within a predetermined time after completing the writing for 1 bit. In this case, the suppressing unit may be a delay circuit for delaying an input of the writing instruction to the charge unit for at least a time equivalent to a discharge time for the signal line.

[0016] Another semiconductor integrated circuit includes a charge unit for charging a signal line corresponding to each 1 row in response to an input of a writing instruction for each bit of a memory cell arranged in n rows by m columns and charging a signal line corresponding to a next row after writing on all bits for one column is completed. The semiconductor integrated circuit performing writing on each 1 bit sequentially in each of bits for 1 column corresponding to the signal line charged by the charge unit. Further, the semiconductor integrated circuit includes a delay unit for differentiating timing for completing writing for 1 bit and timing for changing an address indicating a cell to be written for a time equivalent to a time for charging at least the signal line.

[0017] The above-described charge unit comprises a counter for starting an count operation in response to an input of the writing instruction, a column decoder for decoding a count value of the counter, a switching element for charging the signal line by connecting a predetermined power supply to the signal line after turned ON depending on a decoding result by the decoder, and a row decoder for specifying each 1 bit sequentially for 1 row of bits corresponding to the signal line charged when the switching element is turned ON.

[0018] An ink cartridge according to the present invention has the above-described semiconductor integrated circuit, for storing at least a remained amount of ink on the memory cell.

[0019] An inkjet recording device according to the present invention has the above-described ink cartridge for printing desired image information by using ink supplied from the ink cartridge.

Brief Description of the Drawings

[0020]

- Fig. 1 is a circuit diagram showing one example of a discharge circuit within a semiconductor integrated circuit according to the present invention;
- Fig. 2 is a functional block diagram for describing the internal construction of a semiconductor integrated circuit using the discharge circuit in Fig. 1;

- Fig. 3 is a timing chart for describing a read-out operation on the semiconductor integration
- Fig. 4 is a timing chart for describing a write-in operation on the semiconductor integrated
- Fig. 5 is a timing chart showing an operation of each of the parts in Fig. 1;
- Fig. 6 is a waveform diagram showing the state of charging/discharging of a parasitic capacity;
- Fig. 7 is a diagram showing a circuit substrate on which the semiconductor integrated circuit shown in Fig. 1 is mounted;
- Fig. 8 is a diagram showing the condition where the circuit substrate shown in Fig. 7 is mounted on an ink cartridge;
- Fig. 9 is a diagram showing an overview of an inkjet printer to which the ink cartridge shown in Fig. 8 is attached;
- Fig. 10 is a diagram showing the construction of a carriage shown in Fig. 9.
- Fig. 11 is a diagram showing the condition before an ink cartridge is attached to a holder;
- Fig. 12 is a diagram showing the condition where an ink cartridge is attached to a holder;
- Fig. 13 is a block diagram showing one example of a conventional discharge circuit; and
- Fig. 14 is a diagram for describing an operational example of the discharge circuit shown in Fig. 13.

Best Mode for Carrying Out the Invention

[0021] Next, an embodiment of the present invention will be described with reference to drawings. In each of drawings referenced in the description below, like parts are indicated by like reference numerals.

[0022] Fig. 1 is a circuit diagram showing the structure of an example of a discharge circuit within a semiconductor integrated circuit according to the present invention. The discharge circuit shown in the figure is different from the conventional circuit shown in Fig. 13, and a delay circuit 10 is inserted before the address counter 2. Further, an AND gate 109 is provided instead of buffer 108.

[0023] In the circuit of this structure, input of a write signal WR to the address counter 2 can be delayed by the delay circuit 10. That is, by delaying the update timing of an address after writing, it is arranged to perform

discharge from a column selecting transistor through the AND gate 109. More specifically, the discharge is performed through a transistor in the output stage of the AND gate 109.

[0024] In general, in this type of semiconductor integrated circuit, there is a margin to address updating at a trailing edge. However, like the present circuit, when the address counter 2 that is automatically incremented is built in, the charges as described above remain unless the discharge time is long enough. Thus, in the present circuit, the transition timing of the write signal and the address updating timing are different. More specifically, the discharge time can get a margin by delaying the address updating timing for a predetermined amount of time with respect to the transition timing of the write signal.

[0025] In this case, the discharge speed depends on the driving capability (equivalent resistance), and the delay time can be calculated as the product of an equivalent resistance R and a capacity Cx, that is, a time constant. Further, in order to reduce the size of the circuit as much as possible, it is convenient to keep the insertion of the delay circuit 10 at one point. Thus, in this embodiment, it is provided at a position before the address counter 2 (input side).

[0026] Fig. 2 is a functional block diagram for describing the internal structure of a semiconductor integrated circuit using the discharge circuit shown in Fig. 1. As shown in the figure, semiconductor integrated circuit 1 includes an address counter 2 for performing a count operation, a row decoder 3 and a column decoder 4 for decoding a count value in the address counter 2 in order to create an address, the memory cell array 5 for storing data, a write/read control circuit 6 for controlling a latch circuit 7 and a buffer B depending on writing into or reading out of the memory cell array 5, the latch circuit 7 controlled by the write/read control circuit 6 to assume a latch status or a through status, the input/output control circuit 8 for controlling input and output of data to the memory cell array 5, AND gates G1 to G3, and the delay circuit 10 for delaying write signals. Further, the semiconductor integrated circuit 1 is provided with external terminals P1 to P6.

[0027] The count value of the address counter 2 is initialized to a predetermined value based on the inverted signal of a chip-select input signal CS input to the external terminal P1. Further, the address counter 2 creates updated address data based on a signal input from the AND gate G1. The created address data is input to the row decoder 3 and the column decoder 4.

[0028] The column decoder 4 selects the column including the desired memory cell in the memory cell array 5 based on address data input from the address counter 2. Similarly, the row decoder 3 selects the row including the desired memory cell in the memory cell array 5 based on the address data input from the address counter 2.

[0029] The memory cell array 5 is formed by arranging

a plurality of memory cells in a matrix. Each memory cell in an addressed row is turned to an ON status by a select signal from the row decoder 3, while a select signal from the column decoder 4 enables information stored in the memory cell to be read and written. In this case, it is assumed that the memory cell array 5 is formed by non-volatile memory cells.

[0030] The write/read control circuit 6 determines whether writing or reading is performed on the memory cell array 5 based on the chip-select control signal CS input to the external terminal P1 and signals output from an AND gate G2 or G3. The output of the AND gate G2 is write signal WR. The latch circuit 7 outputs read data of the memory cell array 5, which is output from the input/output control circuit 8, to an external terminal P6 after keeping it for a predetermined period of time based on a control signal from the write/read control circuit 6. The latch circuit 7 performs either a latch operation or a through operation depending on the output of the write/read control circuit 6. The latch circuit 7 performs the latch operation when the output of the write/read control circuit 6 is at the low level, whereas the latch circuit 7 performs the through operation when the output of the write/read control circuit 6 is at the high level. The latch operation is an operation for maintaining the output status. The through operation is an operation for sending out the input signal as an output signal as it is.

[0031] The input/output control circuit 8 writes, into the memory cell array 5, data input to the external terminal P6, or conversely, outputs read-out data to the external terminal P6 through the latch circuit 7. The input/output control circuit 8 is operated by the write signal WR. The write signal WR is input to the address counter 2 after being delayed by the delay circuit 10. The delay time of the delay circuit 10 is a time substantially equal to the time for discharging charges accumulated on the above-described parasitic capacity Cx. According to the structure above, data writing is performed on the memory cell array 5. The written data is, for example, a remaining amount of ink. By writing the amount of remaining ink, the remaining amount of ink can be always monitored.

[0032] The AND gate G1 outputs, to the address counter 2 and the AND gate G2 or G3, a signal which is the conjunction of the chip-select control signal CS input via the external terminal P1 and a clock input signal CK input via the external terminal P2.

[0033] The AND gate G2 outputs, to the write/read control circuit 6, a signal which is the conjunction of the output signal from the AND gate G1 and a write/read input signal W/R from the external terminal P3. On the other hand, the AND gate G3 outputs, to the write/read control circuit 6, a signal which is the conjunction of the output signal from the AND gate G1 and the inverted signal of the write/read input signal W/R from the external terminal P3.

[0034] More specifically, when the input signal from the AND gate G1 is "L", the outputs of the AND gates

G2 and G3 are both "L". On the other hand, when the input signal from the AND gate G1 is "H", and a write/read input signal W/R is "H", the output of the AND gate G2 is "H" while the output of the AND gate G3 is "L". Conversely, if the write/read input signal W/R is "L", the output of the AND gate G2 is "L" while the AND gate G3 is "H". In this way, the AND gates G2 and G3 are arranged not to vary their outputs even if the write/read input signal W/R varies.

[0035] The external terminal P1 is a terminal for inputting the chip-select input signal CS, that is a control signal STB for selecting a specific device when a plurality of devices exist at the same time, for initializing the address counter 2, and for shifting the operation mode. That is, the external terminal P1 in this embodiment is a terminal used both as a control terminal for initializing an address counter and as a control terminal for shifting the operation mode.

[0036] The external terminal P2 is a terminal for inputting the clock input signal CK that is a reference for the semiconductor integrated circuit 1 to operate. The external terminal P3 is a terminal for inputting the write/read input signal W/R for specifying an access operation on the memory cell array 5 built in the semiconductor integrated circuit 1.

[0037] The external terminals P4 and P5 are input terminals for applying operational voltage at a high potential voltage level V_{DD} and at a low potential voltage level V_{SS} for the semiconductor integrated circuit 1 to operate. The external terminal P6 is an input/output terminal for inputting data to be actually written into the memory cell array 5 built in the semiconductor integrated circuit 1 and/or for outputting data read out from the memory cell array 5.

[0038] Next, operations of the semiconductor integrated circuit according to this embodiment will be described with reference to Figs. 3 and 4.

[0039] Fig. 3 is a timing chart for describing a readout operation on the semiconductor integrated circuit. Fig. 2 shows the chip-select control signal CS, the write/read input signal W/R, the clock CLOCK, the count values of the address counter 2, and the input/output signals I/O at the external terminal P6 in Fig. 2. When the readout is performed on the memory cell array 5, "L" is applied to the external terminal P1, first of all, to initialize the address counter 2. Next, "H" is applied to the external terminal P1, and clock pulses for an intended readout start address are input via the external terminal P2. During inputting the clock pulses, "L" for specifying the readout is applied as a write/read input signal W/R to the external terminal P3.

[0040] The address corresponding to data to be read is output in a period when the clock-input signal CK is turned to "L". During the period when the clock input signal CK is "H", the data is maintained since it is latched within the latch circuit 7 at the leading edge. At the trailing edge, the address is incremented, and data for the next address is output from the external terminal P6.

[0041] Fig. 4 is a timing chart for describing a write operation on the semiconductor integrated circuit, for example. Fig. 4 shows the chip-select control signal CS, the write/read input signal W/R, the clock CLOCK, the count values of the address counter 2, and the input/output signals I/O at the external terminal P6. When a write is performed on the memory cell array 5, "L" is applied to the external terminal P1 in a condition where the write/read input signal W/R is "L" in order to initialize the address counter 2. Next, "H" is applied to the external terminal P1, and clock pulses for an intended write start address are input via the external terminal P2. Then, during the write operation, "H" for specifying the write is applied as the write/read input signal W/R to the external terminal P3.

[0042] Next, a process for instructing the semiconductor integrated circuit 1 to perform memory initialization and operation mode shifting will be described. As described above, when "L" is applied to the external terminal P1, the address counter 2 is initialized. This is a procedure absolutely required for initialization of the semiconductor integrated circuit 1 and the same is done for circuits other than the memory cell array 5, including the write/read control circuit 6. Here, the external terminal P6 is open (high-impedance condition).

[0043] In addition, when "L" is applied to the external terminal P1, the stand-by signal STB for the operation mode shifting is turned to "L", and the operation mode of the semiconductor integrated circuit 1 is shifted to the stand-by mode. When the operation mode of the semiconductor integrated circuit 1 is shifted to the stand-by mode, operation of parts where current flows steadily is terminated to achieve a reduction of the current consumption. More specifically, the sense amplifier provided within the input/output control circuit 8, for example, always needs current flow. Therefore, in order to suppress power consumption in the present circuit in the stand-by mode, the source voltage to be supplied to the input/output control circuit 8 is turned to OFF.

[0044] Thus, in this embodiment, when the chip-select input signal CS is "L", that is, when the external terminal P1 is in an unselected condition, the address counter 2 is initialized and the semiconductor integrated circuit 1 is shifted to the stand-by mode. Since these instructions are controlled by inputs to the external terminal P1, that is a dual-usage terminal, the memory initialization function and the function for shifting to the stand-by mode are provided, achieving a reduction of the number of external terminals. Further, the control terminal for the memory initialization and the control terminal for operation mode control are combined to one dual-usage terminal, which makes the control easier.

[0045] In this case, the functions for the circuit block initialization and the operation mode shifting may be arranged such that the address counter 2 is initialized and the semiconductor integrated circuit 1 is shifted to the stand-by mode when the logical operation between the input to the external terminal P1 and the input to other

terminals is in the unselected condition.

[0046] Fig. 5 is a timing chart showing timing for address changes for write signals in the conventional circuit and the present circuit, respectively. Referring to the figure, voltage of the data wire DW is changed synchronously with the timing of leading and trailing edges of the write signals WR. In this example, the voltage alternates between 0 volt and 15 volt. In the conventional circuit, since the delay circuit 10 is not provided, the content at an address ADBS1 is changed synchronously with the trailing edge of the voltage waveform of the data wire DW. Thus, the address is changed before discharge of integrated charges in the parasitic capacity is completed, and wrong writing may be performed.

[0047] On the other hand, since the delay circuit 10 is provided in the present circuit, the content of an address ADRS2 is changed with a small delay compared to the case of the address ADRS1. Here, if the delay time is defined as a time enough for completing the discharge of charges integrated in the parasitic capacity, the address is changed after the completion of the discharge. Therefore, in the present circuit, wrong writing is not caused. In other words, by suppressing a change in address for a predetermined period of time, the wrong writing can be prevented.

[0048] In Fig. 6, a charging/discharging waveform in the conventional circuit and a charging/discharging waveform in the present circuit are shown. With respect to the voltage change on the data wire DW, charges integrated in the parasitic capacity are discharged slowly in a node A of the conventional circuit, as shown in the figure. Therefore, the address is changed before the completion of the discharge, and wrong writing may occur.

[0049] On the other hand, in the present circuit, with respect to the voltage change on the data wire DW, charges integrated in the parasitic capacity are discharged quickly in a node A'. Therefore, the address is changed after the completion of the discharge, and the wrong writing does not occur.

[0050] As described above, since a delay circuit is provided in the present circuit, the address change is suppressed for a predetermined period of time. Thus, since the time for discharging charges accumulated in the parasitic capacity can be reserved, and since the address is changed after the discharge is completed, wrong writing does not occur.

[0051] Figs. 7(a) to 7(e) are diagrams showing a circuit substrate on which the semiconductor integrated circuit according to this embodiment is provided. As shown in Fig. 7(a), contacts 12 are formed on a surface side of a circuit substrate 11. These contacts 12 are connected to the above-described external terminals P1 to P6. Further, as shown in Fig. 7(b), the semiconductor integrated circuit 1 is implemented or mounted on the back side of the circuit substrate 11.

[0052] As shown in Fig. 7(c), the circuit substrate 11 is in a substantially rectangular plate form. The circuit

substrate 11 is provided with a notch portion 11 a and a hole portion 11 b. They are used for positioning the circuit substrate 11 when mounted on an ink-cartridge described below. Further, as shown in Fig. 7(d), a recess 12a may be provided on the surface of each of the contacts 12 provided on the circuit substrate 11. Providing the recess 12a, as shown in Fig. 7(e) improves the electric connection condition with a contact 29 provided on the ink cartridge described below.

[0053] Figs. 8(a) and (b) are diagrams for showing the circuit substrate shown in Fig. 7 attached to an ink cartridge. Fig. 8(a) shows a case where the circuit substrate 11 is mounted on a black ink cartridge 20 accommodating black ink. The black ink cartridge 20 accommodates, in a container 21 formed as a substantially rectangular parallelepiped, a porous body, not shown, impregnated with black ink, and the top surface is sealed by a lid body 23. On the bottom surface of the container 21, an ink supplying outlet 24 is formed at a position facing to an ink supplying needle when attached to a holder. In addition, an overhang portion 26 associated with a projection of a lever of the body is formed integrally at an upper edge of a vertical wall 25 at the side of the ink supplying outlet. The overhang portions 26 are formed on both sides of the wall 25 separately, and each has a rib 26a. Further, a triangular rib 27 is formed between a bottom surface and the wall 25.

[0054] The circuit substrate 11 is attached to the side where the ink supplying outlet of the horizontal wall 25 is formed. The circuit substrate 11 has a plurality of contacts on a surface facing the contacts of the body and has a memory element on the back surface. In addition, projections 25a and 25b and overhang portions 25c and 25d are formed on the horizontal wall 25 in order to position the circuit substrate 11.

[0055] On the other hand, Fig. 8(b) shows a case where the circuit substrate 11 is attached to a color ink cartridge accommodating color ink. The color ink cartridge 30 accommodates, in a container 31 formed as a substantially rectangular parallelepiped, a porous body, not shown, impregnated with ink and sealed with a lid body 33 on the upper surface.

[0056] Five ink accommodating portions accommodating five colors of color ink separately and respectively are sectionally formed inside of the container 31. At the bottom surface of the container 31, an ink supplying outlet 34 is formed for each ink color at a position facing a respective ink supplying needle when attached to the holder. In addition, overhang portions 36 associated with a projection of a lever of the body is formed integrally at an upper edge of a vertical wall 35 at the side of the ink supplying outlet. The overhang portions 36 are formed on the both side of the wall 35 separately, and each has a rib 36a. Further, a triangular rib 37 is formed between a bottom surface and the wall 35. Furthermore, the container 31 has a recess 39 in order to prevent a mis-insertion.

[0057] A recess 38 is formed at a side of the horizontal

wall 35 where an ink supplying outlet is formed such that it is positioned at the center of each cartridge 30 in the width direction, and the circuit substrate 11 is attached here. The circuit substrate 11 has a plurality of contacts on a surface facing to the contacts of the body and has a memory element on the back surface. In addition, projections 35a and 35b and overhang portions 35c and 35d are formed on the horizontal wall 35 in order to position the circuit substrate 11.

[0058] Fig. 9 is a diagram showing an overview of an inkjet printer (inkjet recording device) to which an ink cartridge shown in Fig. 8 is attached. In Fig. 9, a holder 44 for accommodating each of the black ink cartridge 30 shown in Fig. 8(a) and the color ink cartridge 30 shown in Fig. 8(b) is formed in a carriage 43 connected to a driving motor 42 through a timing belt 41. Further, a recording head 45 for receiving the supply of ink from each of the ink cartridges 20 and 30 is provided at a bottom surface position on the carriage 43.

[0059] Ink supply needles 46 and 47 communicating with recording head 45 are provided vertically on the bottom surface of the carriage 43 such that they are positioned at the inner part of the device, that is on the side of the timing belt 41.

[0060] Fig. 10 is a diagram showing the construction of the carriage shown in Fig. 9. As shown in Fig. 10, levers 51 and 52 are mounted rotatably with respect to axes 49 and 50 as fulcrums at the upper edge of a vertical wall 48 closely facing to the ink supply needles 46 and 47 among vertical walls forming the holder 44.

[0061] The wall 53 positioned on the side of free edges of the levers 51 and 52 has a slope portion where the bottom surface side is cut diagonally. Further, contact mechanisms 54 and 55 are provided on the vertical wall 48. The contact mechanisms 54 and 55 are connected to the above-described contacts provided on the circuit substrate 11 in a condition where the ink-cartridge is attached. Thus, ink-cartridge recording can be performed by using ink within the ink cartridge.

[0062] Additionally, a base platform 56 is mounted on the vertical wall 48 of the holder 44. Then, a circuit substrate 57 is mounted on the back surface of the base platform 56. The circuit substrate 57 is electrically connected with the contact mechanisms 54 and 55, resulting in that the circuit substrate 11 and the circuit substrate 57 provided in the ink cartridge are electrically connected.

[0063] Fig. 11 is a diagram showing the condition before the ink cartridge is attached to the holder, while Figs. 12(a) to (c) are diagrams showing conditions where the ink cartridge is attached to the holder. As shown in Fig. 11, when the lever 51 is closed in a condition where the ink cartridge 20 is inserted to the holder 44, the ink cartridge 20 is pressed gradually in a direction of an arrow Y. Here, the condition shown in Fig. 12(a) turns to the condition shown in Fig. 12(c), and the ink supply needle 46 is inserted into of the ink cartridge 20. Ink is supplied from the ink cartridge 20 in a condition where

the ink supply needle 46 is inserted into of the ink cartridge 20 and the ink cartridge 20 is attached to the holder 44 completely, that is, in the condition shown in Fig. 12(c).

[0064] In the condition shown in Fig. 12(c), the contacts 12 provided on the circuit substrate 11 and the contacts 29 on the circuit substrate 57 provided on the side of the holder 44 are electrically connected. Thus, an inkjet printer can read and write data freely to/from the semiconductor integrated circuit 1. More specifically, when the power supply of the printer is ON, "L" is applied to the external terminal P1, while "H" is applied when a read or write operation needs to be performed. It can simplify the logic and contribute to the reduction of the chip size.

Industrial Applicability

[0065] Thus, in this embodiment, there is an effect that, by defining a delay of timing as a time equal to or more than a time required for charge discharging, wrong writing due to residual charges can be prevented.

[0066] In general, several bits including 8 bits and 16 bits are regarded as one word, and this is often handled as a unit for reading and writing. However, in this case, a buffer is needed for storing one word temporally. Thus, the size of a circuit is increased, which is not suitable for being installed in an ink cartridge. Therefore, in the present circuit, reading and/or writing are performed for every 1 bit after dividing one word into every 1 bit. Thus, in the present circuit, a buffer is no longer required for maintaining one word, which can reduce the size of a circuit and allows the installation in the ink cartridge.

[0067] Furthermore, by storing the remaining amount of ink in an ink cartridge, at least, the remaining amount of ink cartridge can be always monitored.

Claims

1. A semiconductor integrated circuit, comprising charge means for charging a signal line corresponding to each 1 row in response to an input of a writing instruction for each bit of a memory cell arranged in n rows by m columns (where n and m are natural numbers and so forth) and charging a signal line corresponding to a next row after writing on all bits for one column is completed, the semiconductor integrated circuit performing writing on each 1 bit sequentially in each of bits for 1 column corresponding to the signal line charged by said charge means, and delay means for delaying an input of said writing instruction to said charge means for at least a time equivalent to a discharge time for said signal line.
2. A semiconductor integrated circuit, comprising charge means for charging a signal line corre-

sponding to each 1 row in response to an input of a writing instruction for each bit of a memory cell arranged in n rows by m columns and charging a signal line corresponding to a next row after writing on all bits for one column is completed, the semiconductor integrated circuit performing writing on each 1 bit sequentially in each of bits for 1 column corresponding to the signal line charged by said charge means, and suppressing means for suppressing a change in the address specifying a cell to be written within a predetermined time after completing the writing for 1 bit.

3. A semiconductor integrated circuit according to claim 2, wherein said suppressing means is a delay circuit for delaying an input of said writing instruction to said charge means for at least a time equivalent to a discharge time for said signal line.
4. A semiconductor integrated circuit, comprising charge means for charging a signal line corresponding to each 1 row in response to an input of a writing instruction for each bit of a memory cell arranged in n rows by m columns and charging a signal line corresponding to a next row after writing on all bits for one column is completed, the semiconductor integrated circuit performing writing on each 1 bit sequentially in each of bits for 1 column corresponding to the signal line charged by said charge means, and delay means for making different the timing for completing writing for 1 bit and the timing for changing the address specifying a cell to be written for a time equivalent to a time for charging at least said signal line.
5. A semiconductor integrated circuit according to any one of claims 1 to 4, wherein said charge means comprises a counter for starting a count operation in response to an input of said writing instruction, a column decoder for decoding the count value of said counter, a switching element for charging said signal line by connecting a predetermined power supply to said signal line after being turned ON depending on the decoding result by said decoder, and a row decoder for specifying each 1 bit sequentially for 1 row of bits corresponding to the signal line charged when said switching element is turned ON.
6. An ink cartridge having the semiconductor integrated circuit according to any one of claims 1 to 5, for storing at least a remaining amount of ink on said memory cell.
7. An inkjet recording device having an ink cartridge according to claim 6 for printing desired image information by using ink supplied from the ink cartridge.

FIG. 1

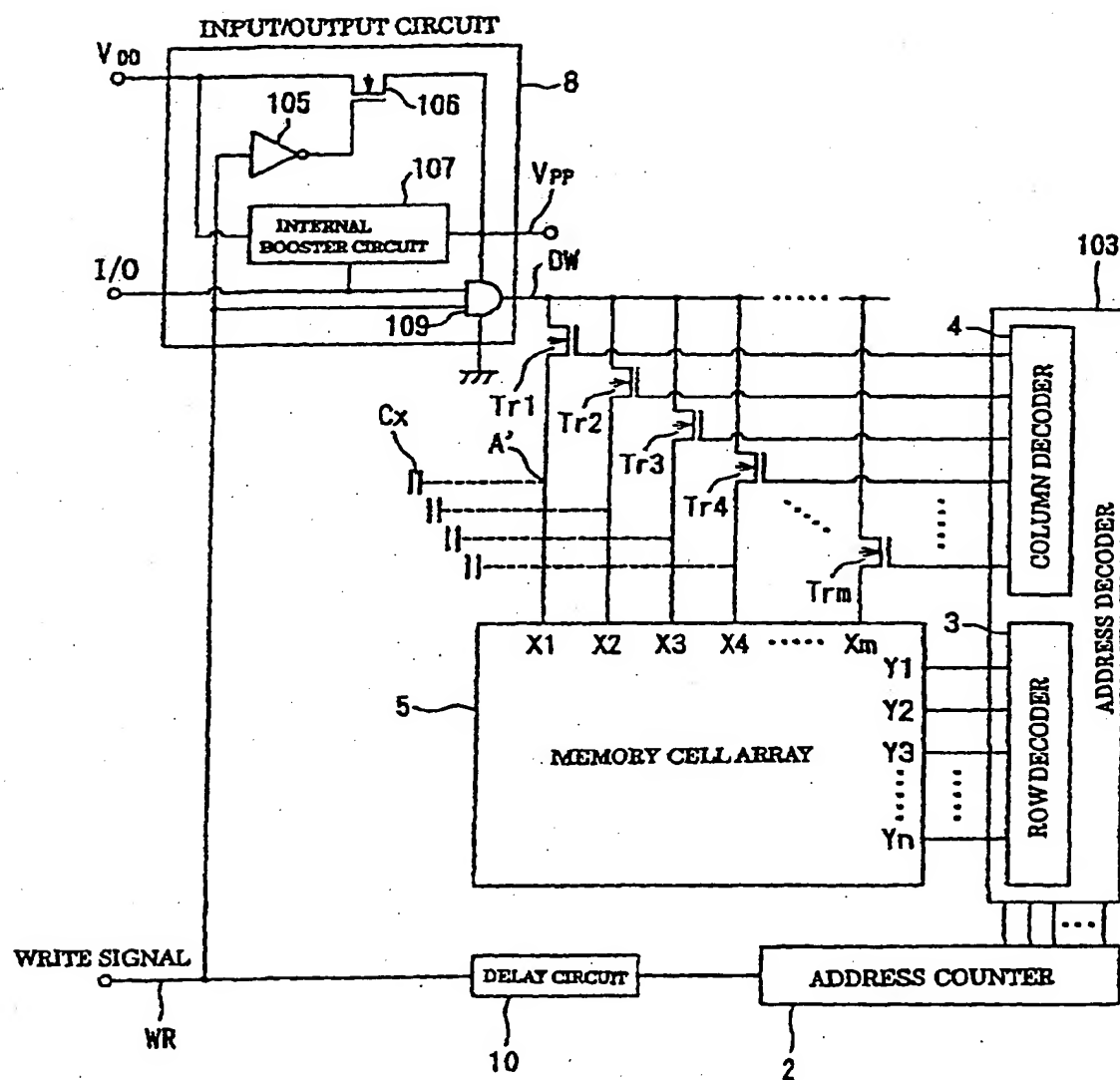


FIG. 2

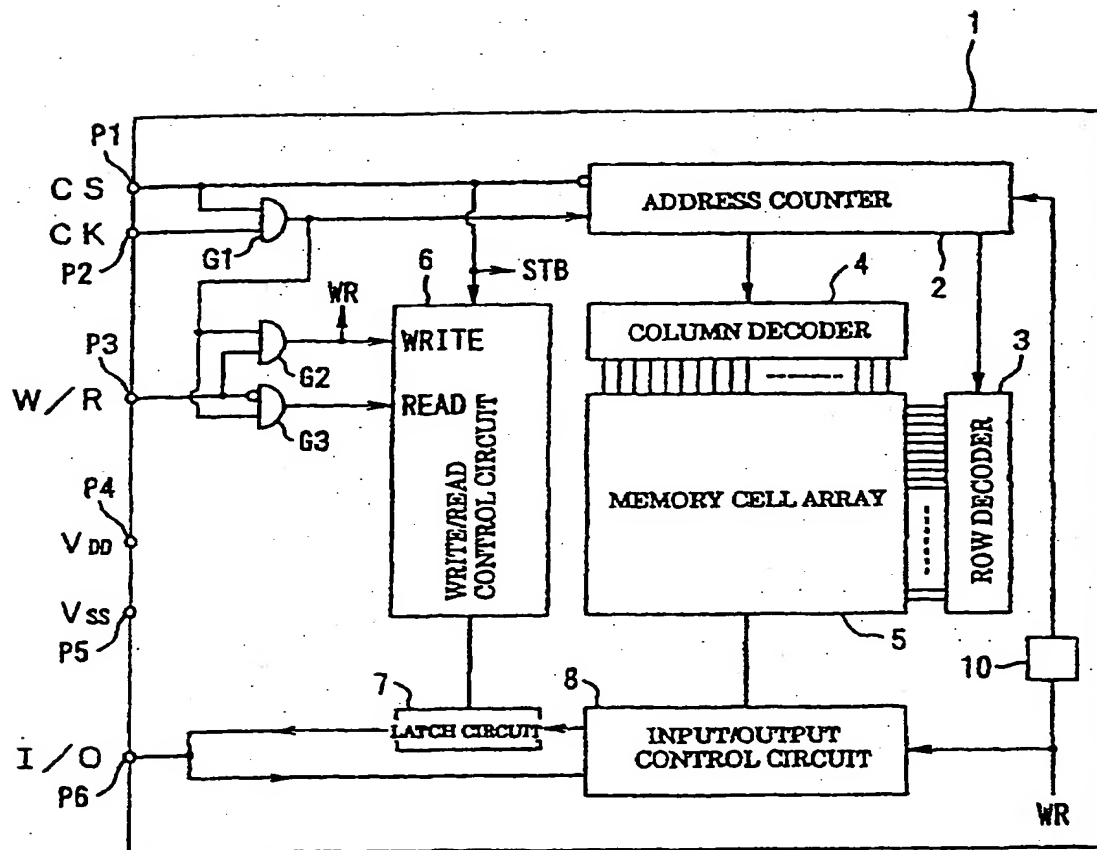


FIG. 3

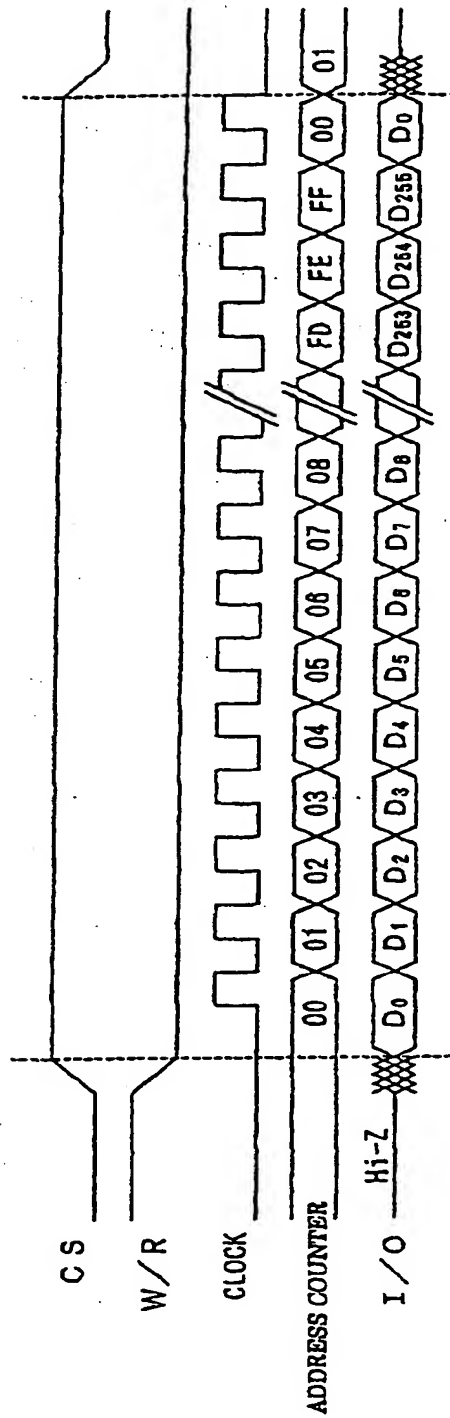


FIG. 4

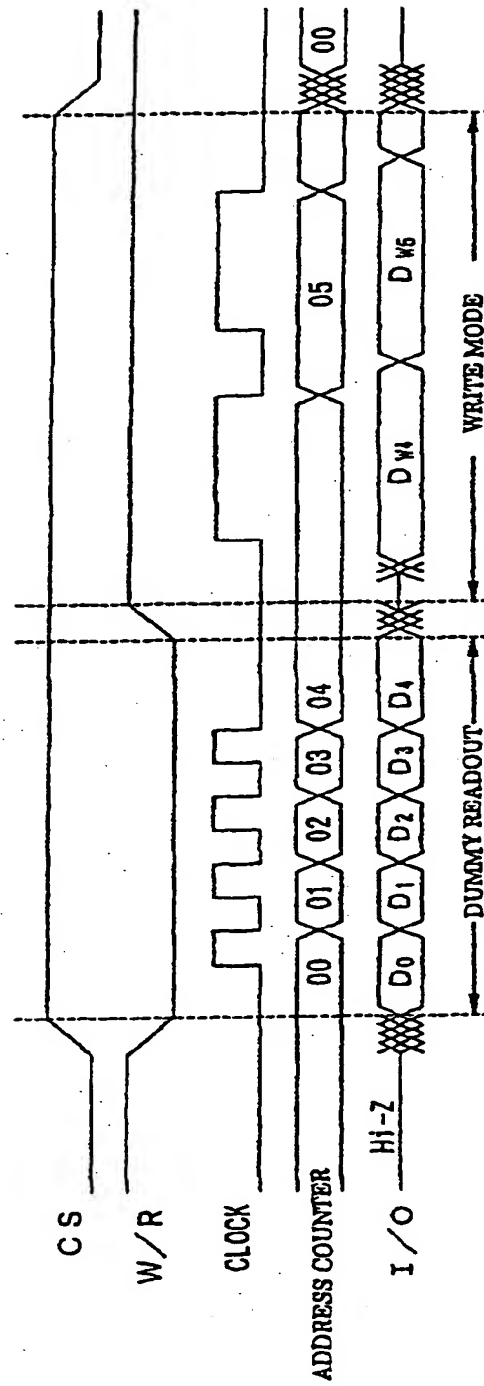


FIG. 5

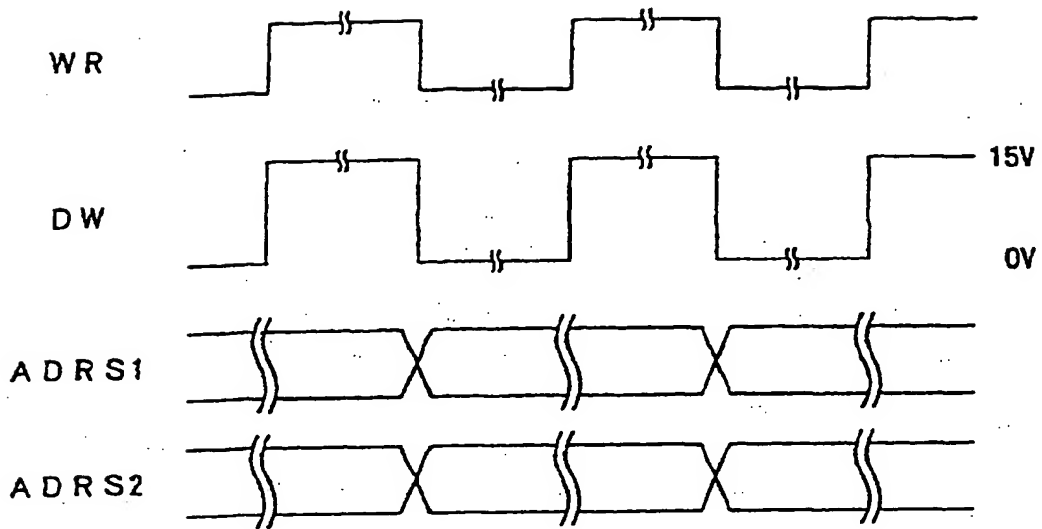


FIG. 6

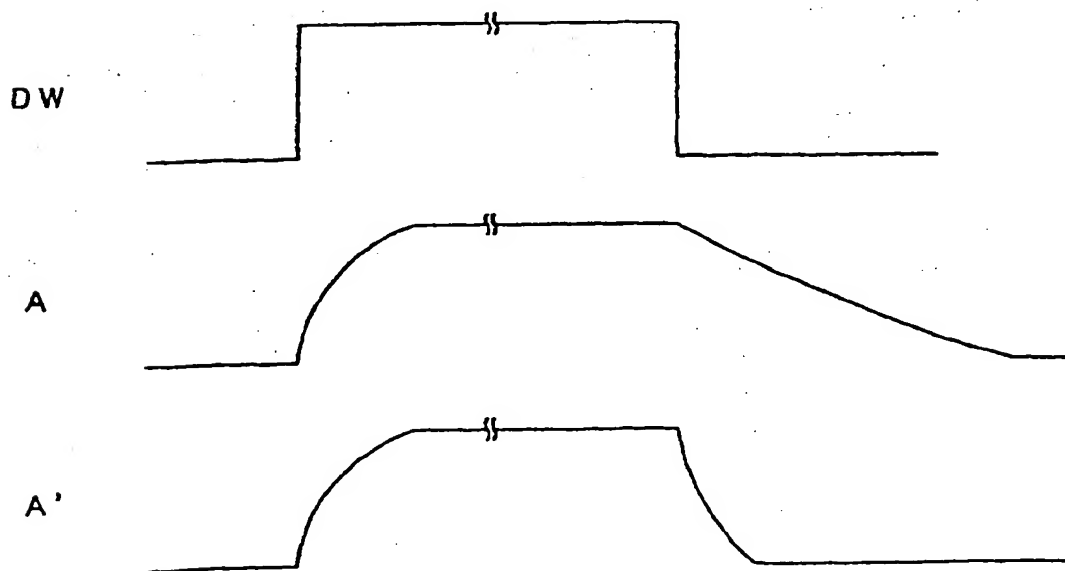


FIG. 7

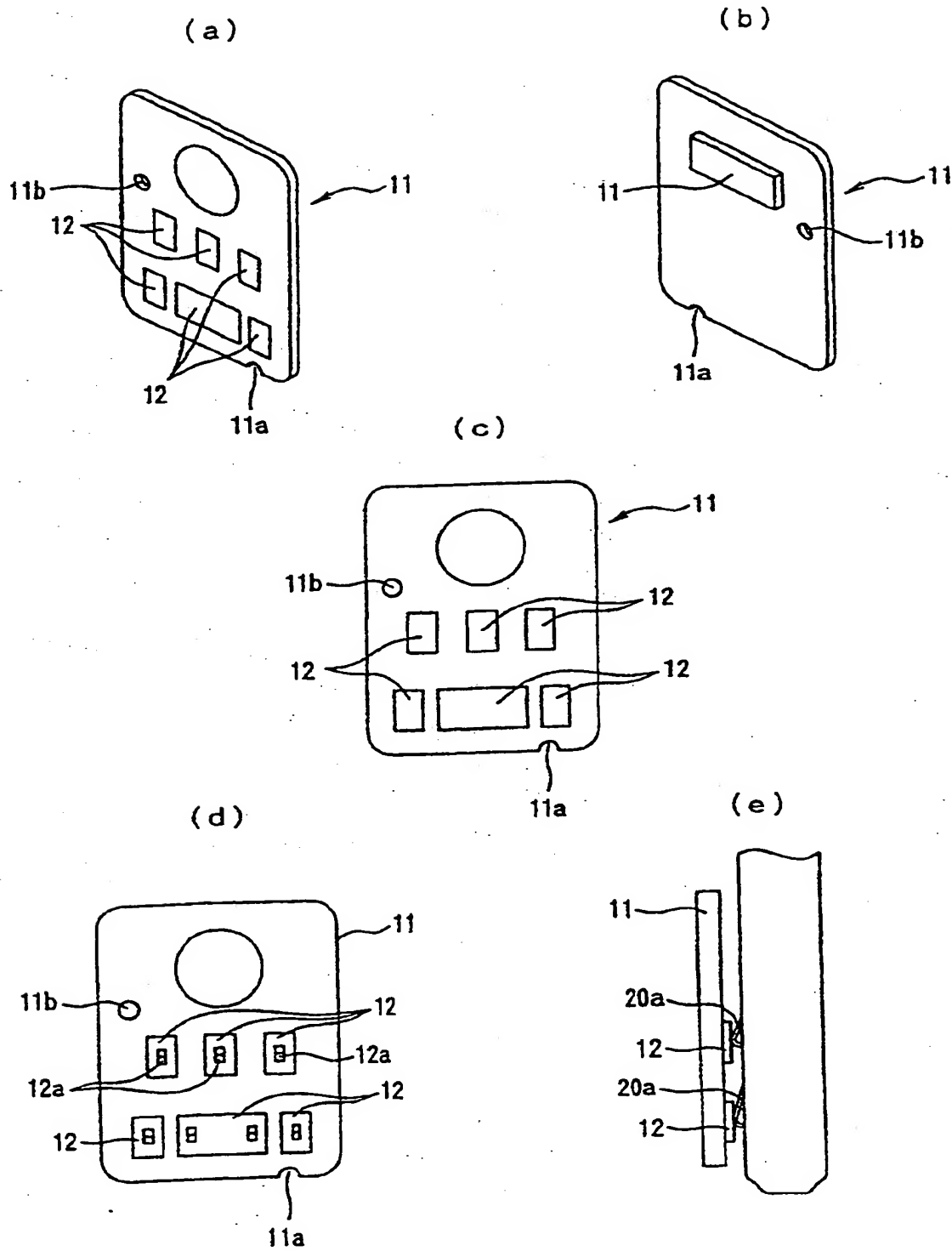


FIG. 8

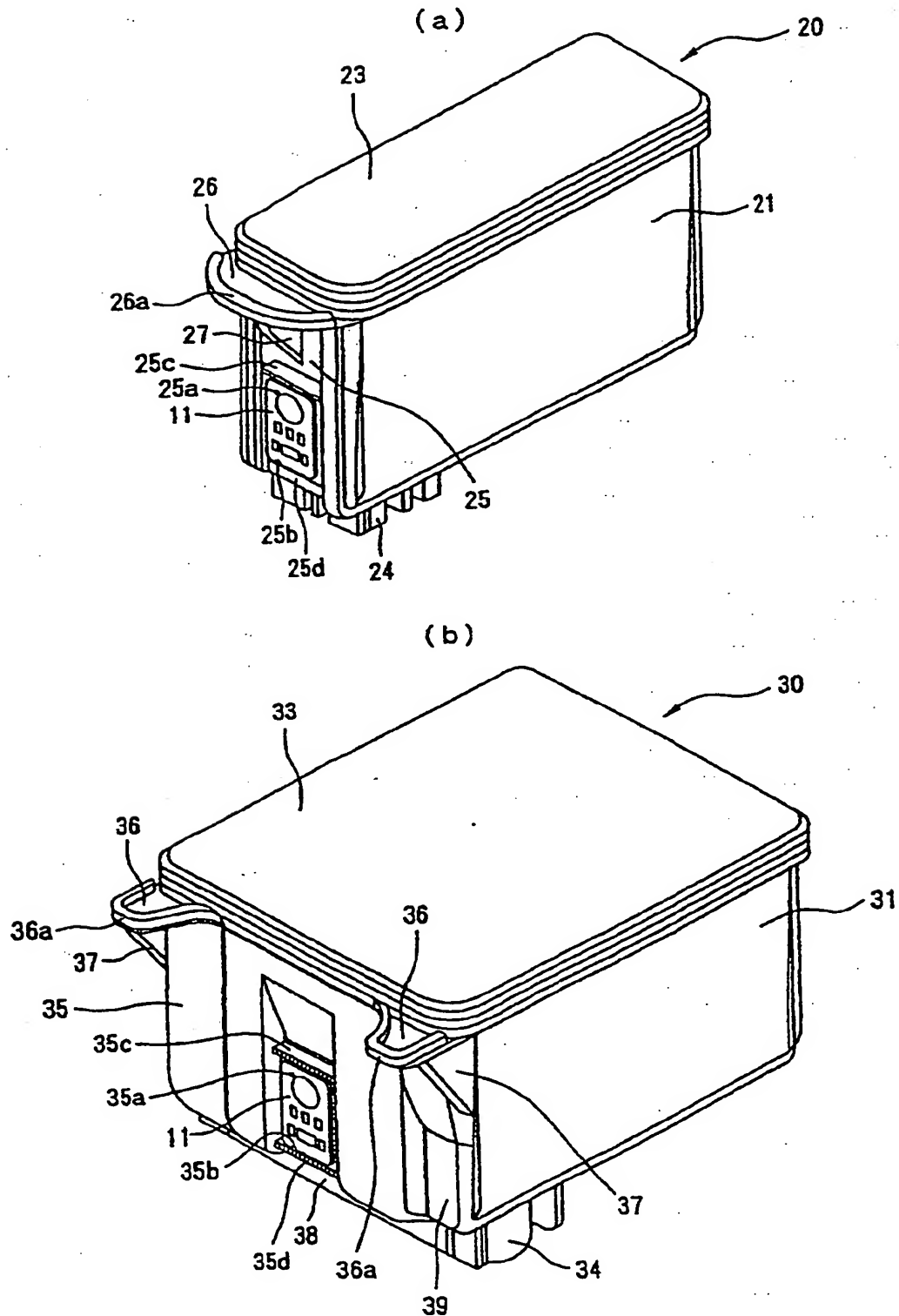


FIG. 9

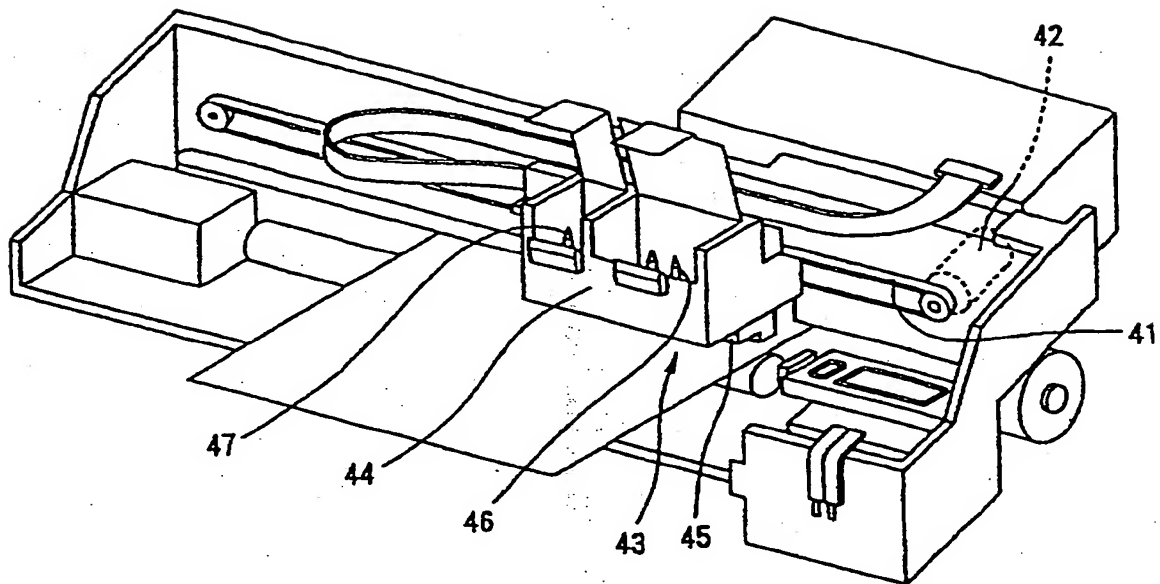


FIG. 10

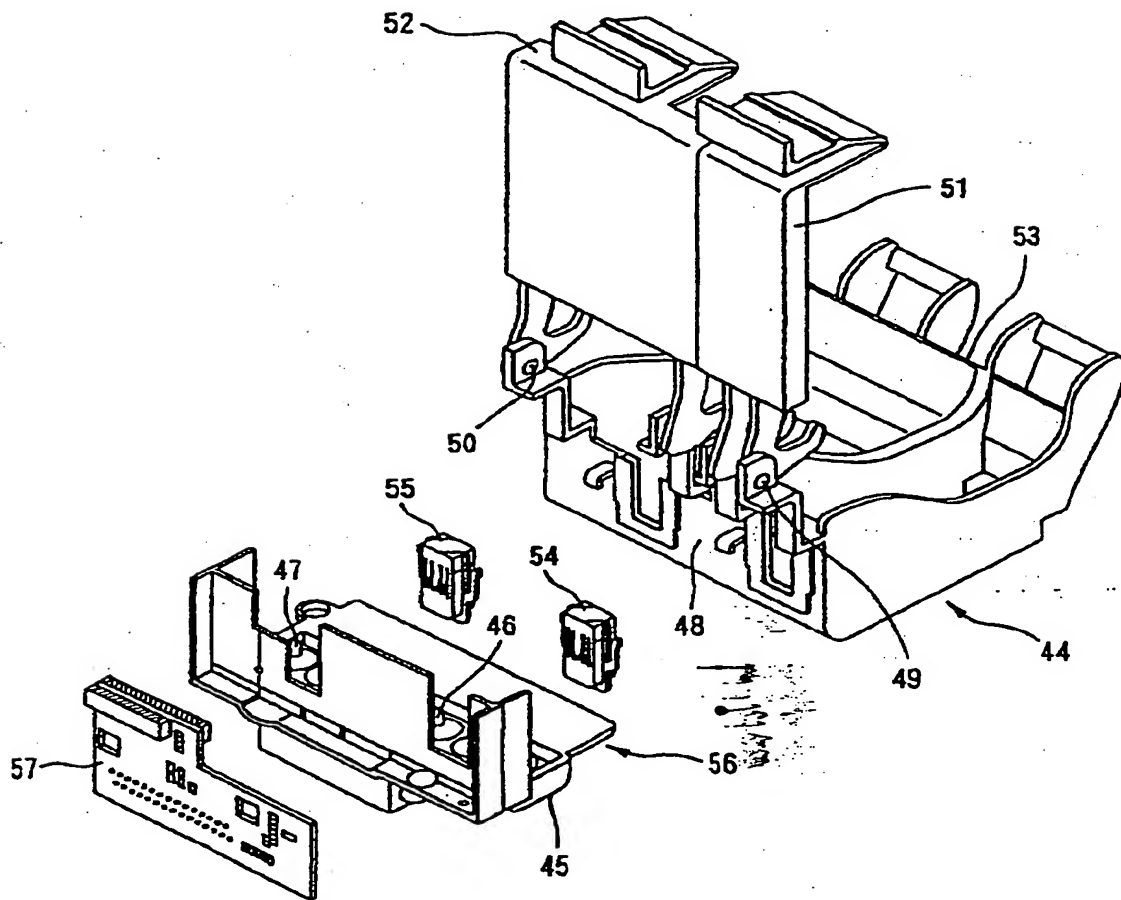


FIG. 11

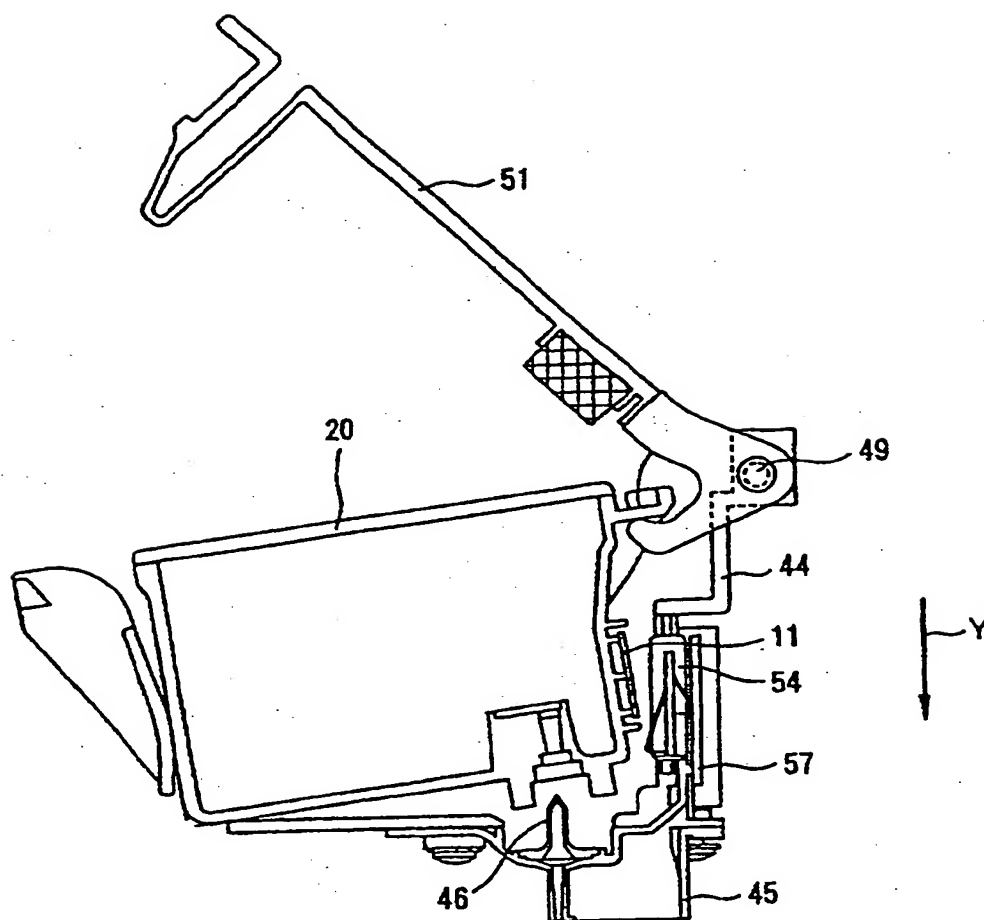


FIG. 12

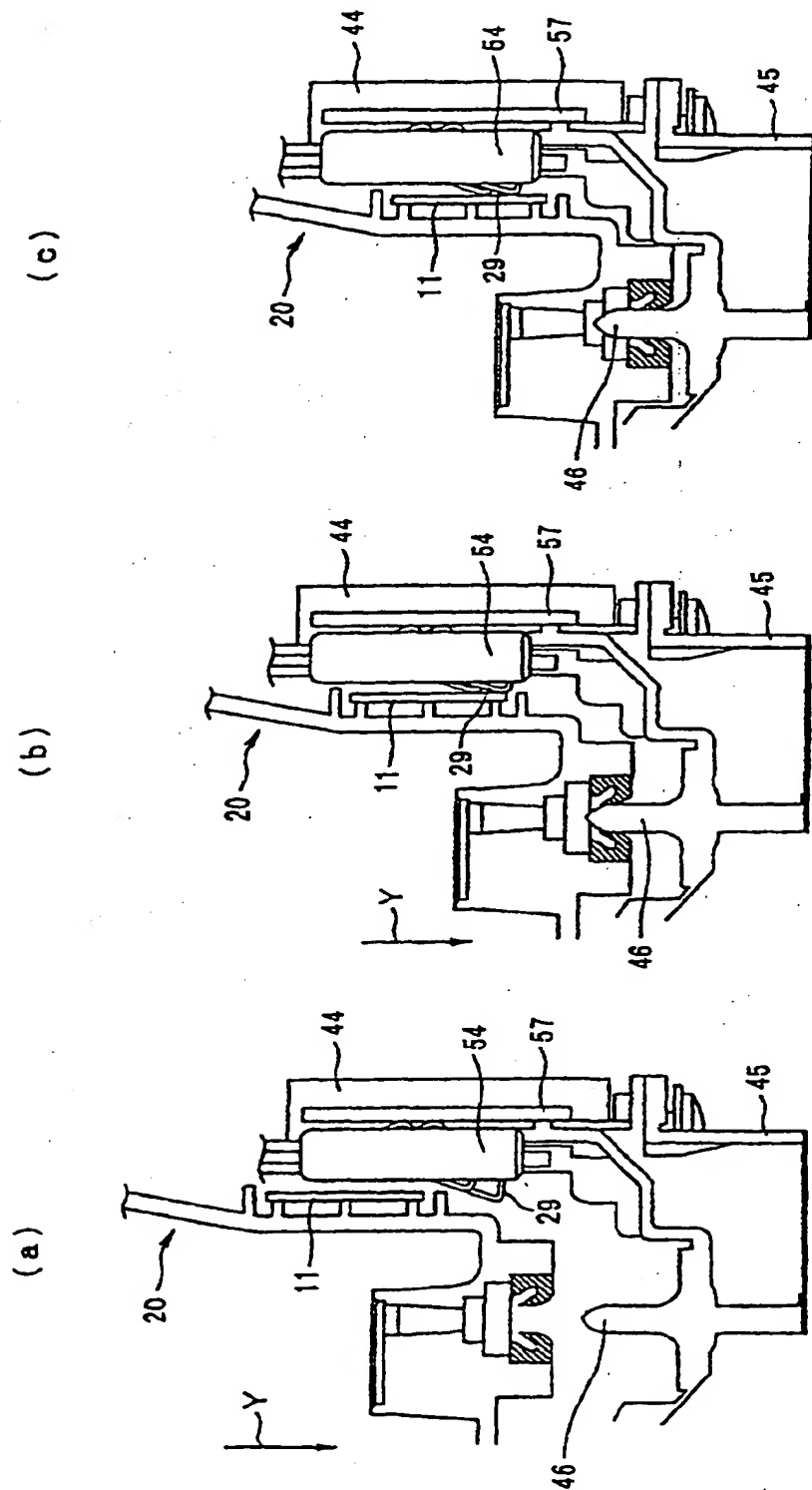


FIG. 13

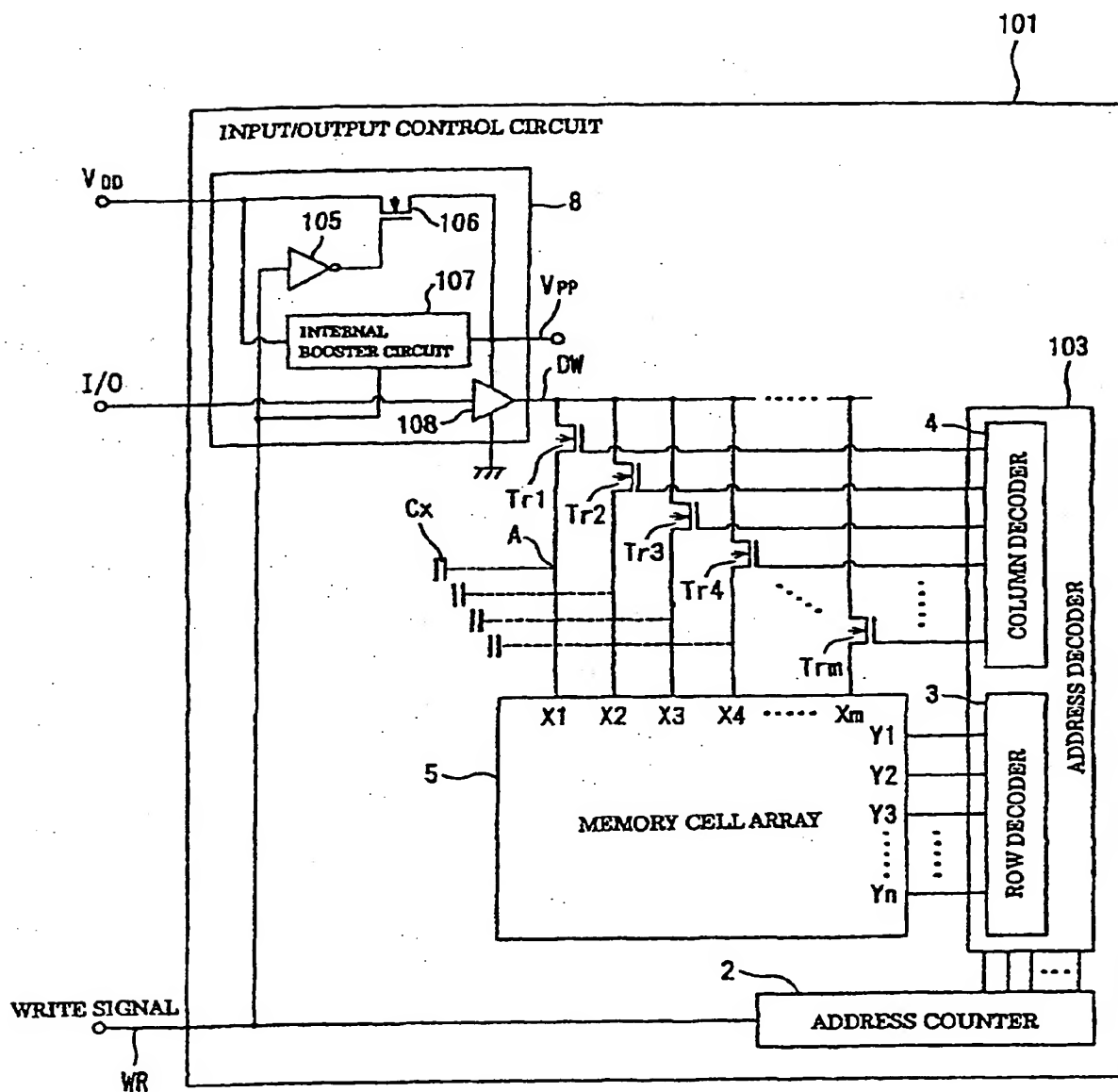
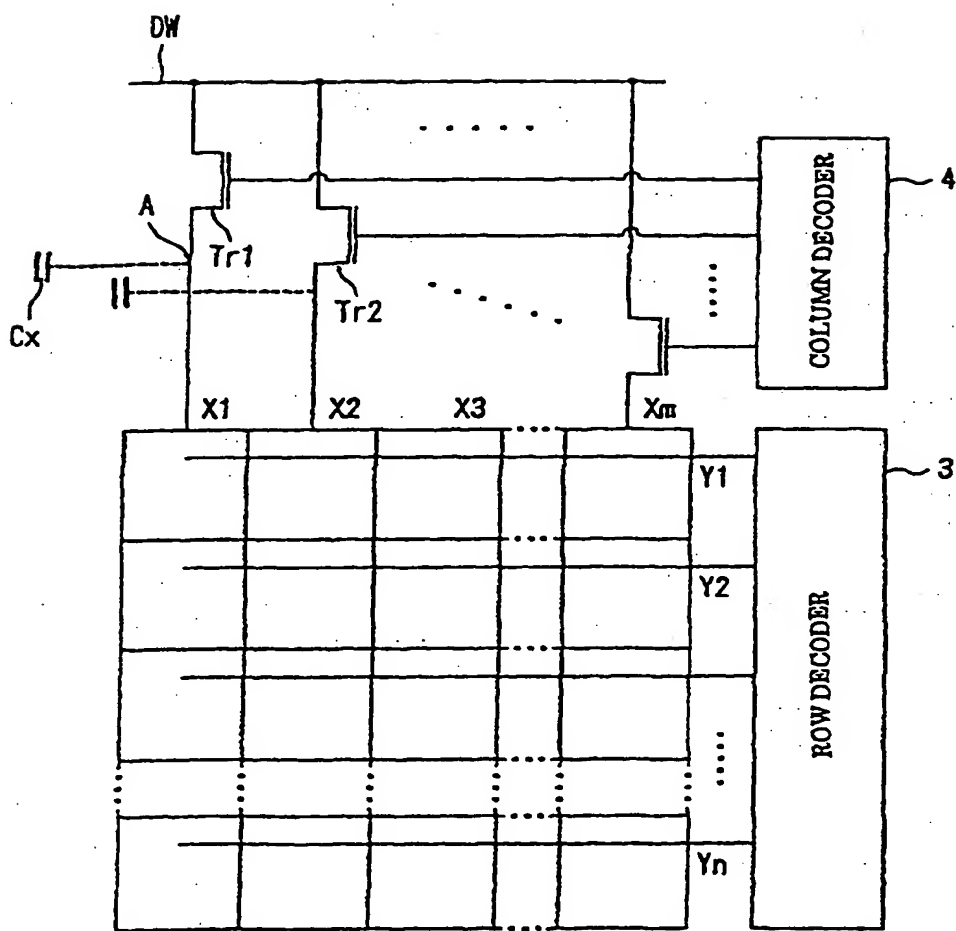


FIG. 14



INTERNATIONAL SEARCH REPORT

International application No.

PCT/JP00/06935

A. CLASSIFICATION OF SUBJECT MATTER Int.Cl. ⁷ G11C17/00, B41J2/175		
According to International Patent Classification (IPC) or to both national classification and IPC		
B. FIELDS SEARCHED Minimum documentation searched (classification system followed by classification symbols) Int.Cl. ⁷ G11C17/00, B41J2/175		
Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched Jitsuyo Shinan Koho 1926-1996 Jitsuyo Shinan Toroku Koho 1996-2000 Kokai Jitsuyo Shinan Koho 1971-2000 Toroku Jitsuyo Shinan Koho 1994-2000		
Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)		
C. DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	JP, 10-69793, A (NEC Kyushu Ltd.), 10 March, 1998 (10.03.98) (Family: none)	1-7
A	JP, 5-301349, A (Canon Inc.), 16 November, 1993 (16.11.93) (Family: none)	6-7
<input type="checkbox"/> Further documents are listed in the continuation of Box C. <input type="checkbox"/> See patent family annex.		
* Special categories of cited documents: "A" document defining the general state of the art which is not considered to be of particular relevance "E" earlier document but published on or after the international filing date "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) "O" document referring to an oral disclosure, use, exhibition or other means "P" document published prior to the international filing date but later than the priority date claimed		"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art "&" document member of the same patent family
Date of the actual completion of the international search 11 December, 2000 (11.12.00)		Date of mailing of the international search report 26 December, 2000 (26.12.00)
Name and mailing address of the ISA/ Japanese Patent Office		Authorized officer
Facsimile No.		Telephone No.

Form PCT/ISA/210 (second sheet) (July 1992)